

- Structure : Silicon Monolithic Integrated Circuit
- Product Series : Power Driver for Compact disc player
- type : **BD8224EFV**
- Feature :
  - 4CH BTL Driver.
  - Employs the HTSSOP-B24PIN power package for compaction.
  - Has a wide dynamic range. ( PowVcc1=8V, RL=8Ω, CH1,2 6.0V (typ.) )
  - The thermal shutdown circuit contained.
  - Switches CH2 input by Control input terminal(CNT).
  - Incorporates mute function by CNT terminal and MUTE terminal.

Absolute maximum ratings(Ta=25 )

| Parameter                   | Symbol            | Limits     | Unit |
|-----------------------------|-------------------|------------|------|
| Power supply voltage        | PowVcc 1,PowVcc 2 | 15         | V    |
| Reset detection terminal    | RSTDET            | PowVcc 2   | V    |
| Input terminal              | IN1,2-1,2-2,3,4   | PowVcc 2   | V    |
| CNT terminal                | CNT               | PowVcc 2   | V    |
| MUTE terminal               | MUTE              | PowVcc 2   | V    |
| Power dissipation           | Pd                | 1.1*1      | W    |
|                             |                   | 4.0*2      |      |
| Operating temperature range | Topr              | -40 ~ +85  |      |
| Storage temperature         | Tstg              | -55 ~ +150 |      |
| Junction temperature        | Tjmax             | +150       |      |

\*1 70mm×70mm×1.6mm, occupied copper foil is less than 3%,one layer substrate(back copper foil 0mm×0mm)  
Reduce power by 8.8mW for each degree above 25 .

\*2 70mm×70mm×1.6mm, occupied copper foil is less than 3%,four layer substrate(back copper foil 70mm×70mm)  
Reduce power by 32.0mW for each degree above 25 .

**Operating conditions**

(Set the power supply voltage taking allowable dissipation into considering.)

|            |                |
|------------|----------------|
| PowVcc 1,2 | 4.5 ~ 10 ( V ) |
|------------|----------------|

Please use it with PowVcc 1= PowVcc 2

**Status of this document**

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

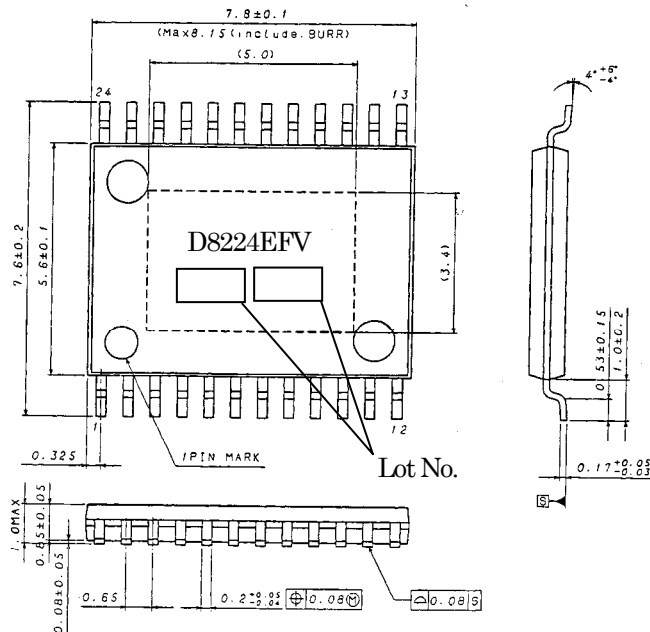
Be careful to handle because the content of the description of this material might correspond to the labor (technology in the design, manufacturing, and use) in foreign country exchange and Foreign Trade Control Law.

A radiation is not designed.

Electrical characteristics ( Unless otherwise noted, Ta=25 , PreVcc=PowVcc=8V, BIAS=2.5V, RL=8 )

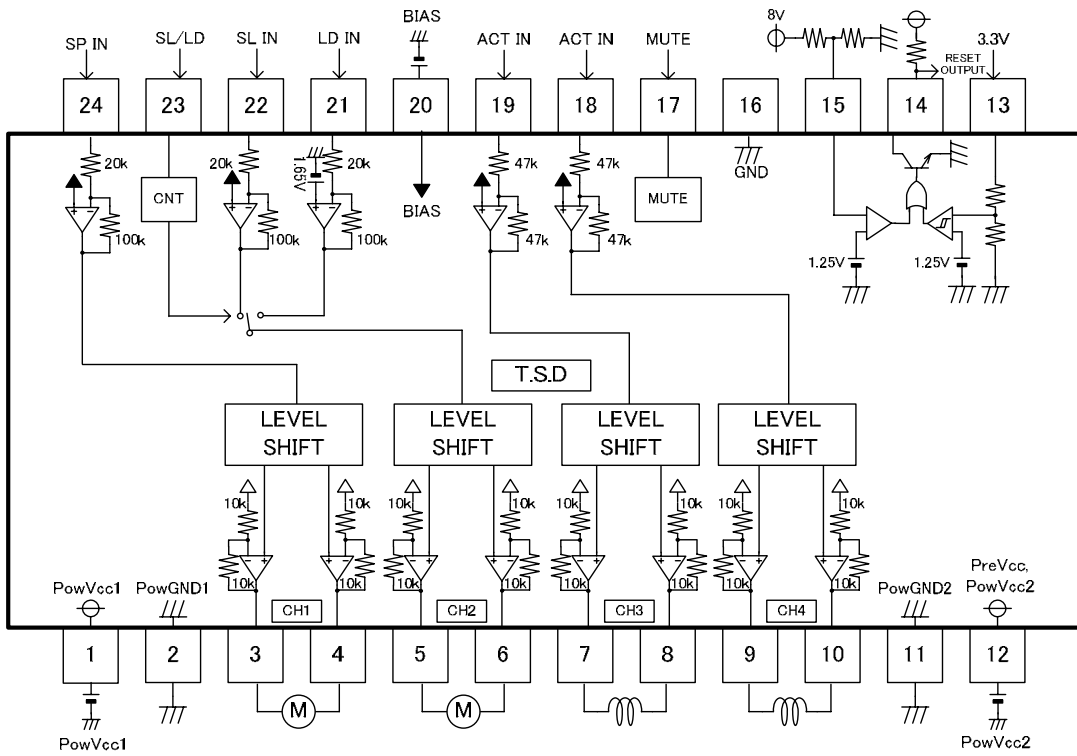
| Parameter                                  | Symbol              | MIN  | TYP  | MAX  | Unit | Condition        |
|--|---------------------|------|------|------|------|------------------|
| Quiescent dissipation current              | IQ                  | 15   | 30   | 45   | mA   | RL=              |
| <b>&lt;Driver&gt;</b>                      |                     |      |      |      |      |                  |
| Output offset voltage (CH3,4)              | V <sub>oof 34</sub> | -50  | 0    | 50   | mV   |                  |
| Output offset voltage (CH1,2)              | V <sub>oof 12</sub> | -100 | 0    | 100  | mV   |                  |
| Maximum output amplitude (CH3,4)           | V <sub>OM 34</sub>  | 4.7  | 5.3  | -    | V    |                  |
| Maximum output amplitude (CH1,2)           | V <sub>OM 12</sub>  | 5.4  | 6.0  | -    | V    |                  |
| Closed circuit voltage gain (CH3,4)        | G <sub>v 34</sub>   | 10.0 | 11.7 | 13.4 | dB   |                  |
| Closed circuit voltage gain (CH1,2)        | G <sub>v 12</sub>   | 24.3 | 26.0 | 27.7 | dB   |                  |
| MUTE terminal low level input voltage      | V <sub>ML</sub>     | -    | -    | 0.5  | V    |                  |
| MUTE terminal high level input voltage     | V <sub>MH</sub>     | 2.0  | -    | -    | V    |                  |
| CNT terminal low level input voltage       | V <sub>CNTL</sub>   | -    | -    | 0.5  | V    |                  |
| CNT terminal high level input voltage      | V <sub>CNTH</sub>   | 2.0  | -    | -    | V    |                  |
| LDIN voltage of terminal ( SLED at input ) | V <sub>LDIN</sub>   | -    | 0.1  | 0.3  | V    | CNT = 'L'        |
| Voltage of internal bias                   | V <sub>BIN</sub>    | 1.53 | 1.65 | 1.77 | V    | CNT = 'H'        |
| <b>&lt;Reset : Vcc&gt;</b>                 |                     |      |      |      |      |                  |
| Reset detection voltage                    | V <sub>DET 1</sub>  | 1.20 | 1.25 | 1.30 | V    | Voltage in Pin15 |
| Detection terminal outflow current         | I <sub>COMP</sub>   | -    | 50   | 150  | nA   |                  |
| <b>&lt;Reset : 3.3V&gt;</b>                |                     |      |      |      |      |                  |
| Reset release voltage                      | V <sub>DET 2</sub>  | 2.75 | 2.95 | 3.15 | V    |                  |
| Hysteresis voltage                         | V <sub>DET</sub>    | 10   | 25   | 40   | mV   |                  |

Package outlines : HTSSOP-B24



HTSSOP-B24(UNIT : mm)

Block diagram



T.S.D : Thermal Shut-Down

Pin description

| No. | Symbol  | Description   | No. | Symbol | Description                           |
|-----|---------|---|-----|--------|---------------------------------------|
| 1   | PowVcc1 | CH1,2 power supply terminal                                       | 13  | RSTIN  | Detection power supply input terminal |
| 2   | PowGND1 | Power GND 1   | 14  | RSTOUT | Reset output                          |
| 3   | VO1(-)  | Driver CH1 negative output  | 15  | RSTDET | Reset detection comparator input      |
| 4   | VO1(+)  | Driver CH1 positive output  | 16  | PreGND | PreGND                                |
| 5   | VO2(-)  | Driver CH2 negative output  | 17  | MUTE   | MUTE terminal                         |
| 6   | VO2(+)  | Driver CH2 positive output  | 18  | IN4    | CH4 input                             |
| 7   | VO3(-)  | Driver CH3 negative output  | 19  | IN3    | CH3 input                             |
| 8   | VO3(+)  | Driver CH3 positive output  | 20  | BIAS   | BIAS input terminal                   |
| 9   | VO4(-)  | Driver CH4 negative output  | 21  | IN2-2  | CH2-2 input                           |
| 10  | VO4(+)  | Driver CH4 positive output  | 22  | IN2-1  | CH2-1 input                           |
| 11  | PowGND2 | Power GND 2   | 23  | CNT    | Control input terminal                |
| 12  | PowVcc2 | Pre block and Reset block , and CH3,4 power supply input terminal | 24  | IN1    | IN1 input                             |

**Cautions in using the IC**

**1. Absolute maximum ratings**

We are careful enough for quality control about this IC. So, there is no problem under normal operation, excluding that it exceeds the absolute maximum ratings. However, this IC might be destroyed when the absolute maximum ratings, such as impressed voltages or the operating temperature range, is exceeded, and whether the destruction is short circuit mode or open circuit mode cannot be specified. Please take into consideration the physical countermeasures for safety, such as fusing, if a particular mode that exceeds the absolute maximum rating is assumed.

**2. Reverse polarity connection**

Connecting the power line to the IC in reverse polarity (from that recommended) will damage the part. Please utilize the direction protection device as a diode in the supply line and motor coil line.

**3. Power supply line**

Due to return of regenerative current by reverse electromotive force, using electrolytic and ceramic suppress filter capacitors (0.1μF) close to the IC power input terminals (Vcc and GND) are recommended. Please note the electrolytic capacitor value decreases at lower temperatures and examine to dispense physical measures for safety. And, for ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

**4. GND line**

Please keep the GND line the lowest potential always, and check the GND voltage when transient voltages are connected to the IC.

**5. Thermal design**

Do not exceed the power dissipation (Pd) of the package specification rating under actual operation, and please design enough temperature margins. This product has exposed the frame to the back side of the package, but please note that it is assumed to use heat radiation efficiency by the heat radiation for this part. Please take the heat radiation pattern on not only the surface of the substrate but also the back of the substrate widely.

**6. Short circuit mode between terminals and wrong mounting**

Do not mount the IC in the wrong direction and displacement, and be careful about the reverse connection of the power connector. Moreover, this IC might be destroyed when the dust short the terminals between them or GND.

**7. Radiation**

Strong electromagnetic radiation can cause operation failures.

**8. ASO (Area of Safety Operation)**

Do not exceed the maximum ASO and the absolute maximum ratings of the output driver.

**9. TSD (Thermal Shut-Down)**

The TSD is activated when the junction temperature (Tj) exceeds Tjmax, and the output terminal is switched to OPEN.

The guarantee and protection of set are not purpose. Therefore, please do not use this IC after TSD circuit operates, nor use it for assumption that operates the TSD circuit.

**10. Capacitor between output driver and GND**

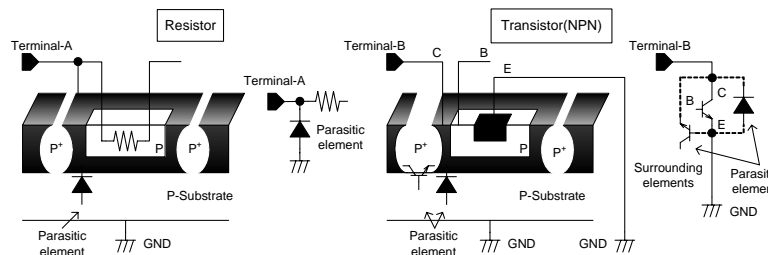
If a large capacitor is connected between the output driver and GND, this IC might be destroyed when Vcc becomes 0V or GND, because the electric charge accumulated in the capacitor flows to the output driver. Please set said capacitor to smaller than 0.1μF.

**11. Inspection by the set circuit board**

The stress might hang to IC by connecting the capacitor to the terminal with low impedance. Then, please discharge electricity in each and all process. Moreover, when attaching or detaching from jig in the inspection process, please turn off the power before mounting the IC, and turn on after mounting the IC, and vice versa. In addition, please take into consideration the countermeasures for electrostatic damage, such as giving the earth in assembly process, transportation or preservation.

**12. Input terminal**

This IC is a monolithic IC, and has P+ isolation and P substrate for the element separation. Therefore, a parasitic PN junction is formed in this P-layer and N-layer of each element. For instance, the resistor or the transistor is connected to the terminal as shown in the figure below. When the GND voltage potential is greater than the voltage potential at Terminal A on the resistor, at Terminal B on the transistor, the PN junction operates as a parasitic diode. In addition, the parasitic NPN transistor is formed in said parasitic diode and the N layer of surrounding elements close to said parasitic diode. These parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the interference of circuit operation, then the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by impressing to input terminals lower voltage than GND (P substrate). Please do not apply the voltage to the input terminal when the power-supply voltage is not impressed. Moreover, please impress each input terminal lower than the power-supply voltage or equal to the specified range in the guaranteed voltage when the power-supply voltage is impressing.



*Simplified structure of IC*

**13. Earth wiring pattern**

If small signal GND and large current GND exist, disperse their pattern. In addition, for voltage change by pattern wiring impedance and large current not to change voltage of small signal GND, each ground terminal of IC must be connected at the one point on the set circuit board. As for GND of external parts, it is similar to the above-mentioned.

**14. About the RESET output**

Please set 14PIN-RESET output terminal and set the voltage which is the pull-up below the voltage of 12PIN:PowVcc2. 14PIN flows and the current flows to protection Di for the surge absorption when the voltage which is the pull-up is higher than the voltage of 12PIN.

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